

ONS000511  
PATENT

S.N. 10/685,094

REMARKS

Claims 1-12 and 14-20 are in the present application.

Claims 2 and 10 are amended to place the claims in condition for allowance as explained further hereinafter.

Claims 1, 8, 11, 15, 16, and 17 are amended to more particularly point out and distinctly claim the inventions.

Claims 9 and 12 are amended to provide proper antecedent basis with amended claim 8.

Claim 13 is cancelled.

Allowable Subject Matter:

The office action states that claims 2-7, 10, and 11 were objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

By this amendment, claim 2 is amended to include the limitations of original claim 1. It is believed that this amendment to claim 2 now places claim 2 in condition for allowance as stated in the Office Action.

By this amendment, claim 10 is amended to include the limitations of original claim 8. It is believed that this amendment to claim 10 now places claim 10 in condition for allowance as stated in the Office Action.

35 USC 112 Rejection:

Claims 2 and 15-20 were rejected under 35 USC 112 as being indefinite. This rejection is respectfully traversed in part and overcome in part by the amendments to the claims.

Claim 2 was rejected because the continuity of the resistor recited in claim 2 was not understood. The rejection continues by stating that the claim fails to clearly associate the resistor with the bias current or the control terminal of the output transistor. Applicants amended claim 2 and it is

ONS000511  
PATENT

S.N. 10/685,094

believed that such amendment may help clarify the issue stated in the Office Action. It is respectfully submitted that amended claim 2 indicates that the resistor is coupled to both receive the bias current from the second current carrying electrode of the J-FET transistor and to couple the bias current to a control electrode of the output transistor. Applicants respectfully submit that these words have very definite meanings and the relationship between the words are clear. Further, applicants respectfully submit that it is not necessary to precisely identify every terminal that is connected to every other terminal but only to identify in a manner that is sufficiently definite to point out the invention. Accordingly, it is respectfully submitted that claim 2 is not indefinite and that the 35 USC 112 rejection thereof should be withdrawn.

The rejection also states that is not understood toward what the "output" is directed as recited in the claims and refers to claim 15. Applicants amended claims 15-17 and some of the amendments include more particularly pointing out the "output". It is believed that such amendments may help clarify the "output" issue stated in the Office Action.

The rejection continues by referring to FIG. 1 and goes into a technical discussion of the operation of one of the example embodiments explained in the "Detailed Description of the Drawings" section of the specification. Applicants refer to page 6, line 17, through page 7, line 27, as one place to refer to for a better technical explanation of the operation of the example embodiment illustrated in FIG. 1, and especially a place to refer to for one of the current flow paths of the current from resistor 13 through resistor 17 to the output node 21 and through diode 29 to output 36, and for another current flow path through transistor 12 through resistor 26 to output node 21 and through diode 29 to output 36. However, it is a well established legal principle that the claims are not a

ONS000511  
PATENT

S.N. 10/685,094

technical description and are not intended to explain how an invention works but is a description that explains the metes and bounds of the invention. Thus, the example embodiments explained in the specification and the example text referred to in the next to last previous sentence do not apply as limitations of the claims but are merely a way to explain the operation of one example embodiment of an implementation of what is set-out in the claims. Further, applicants respectfully submit that the words used in claim 15 are not unclear nor is the definition of them indefinite to render the claims to be indefinite. There are various current flow paths in the example embodiments and the words of the claims may refer to more than one of them and still not be indefinite. Accordingly, it is respectfully submitted that in light of the amendments to claim 15 and the traversal herein, the 35 USC 112 rejection of claim 15 should be withdrawn.

The rejection continues referring to claim 16 that the bias current is unclear and further refers to the operation of transistor 12. Applicants again respectfully submit that the claim is not a detailed engineering explanation of the operation of any of the circuits that are described as different embodiments. If it is unclear as to the operation of one of the example embodiments, applicants refer to the explanation of the description of FIG. 1. For example, the explanation on page 9, line 3 through page 10, line 14. However, it is a well established legal principle that the claims are not a technical description and are not intended to explain how an invention works but is a description that explains the metes and bounds of the invention. Thus, the example embodiments explained in the specification and the example text referred to in the next to last previous sentence do not apply as limitations of the claims but are merely a way to explain the operation of one example embodiment of an implementation of what is set-out in the claims.

ONS000511  
PATENT

S.N. 10/685,094

Referring to the description of the 35 USC 112 rejection of claims 17, 18, and 19, it seems that the confusion is not based on the claims being indefinite but is based on a confusion of the operation of the example embodiments of the "Detailed description of the Drawings", thus, the words of the claims are clear and definite. Applicants respectfully submit that the referred to claims are not indefinite and that the 35 USC 112 rejection thereof should be withdrawn.

The rejection continues referring to the word "coupling" of claim 20 and states that the bias current is not the result of "coupling" components together. Applicants respectfully submit that an examination of the descriptions of the example embodiments described in the specification of the application clearly show that transistor 14 is coupled to input 22 and to node 18, thus, at some point in time a coupling action was performed in order to couple transistor 14 to both receive the input voltage on input 22 and to form the bias current at node 18.

Accordingly, it is respectfully submitted that the 35 USC 112 rejection of claims 15-20 should be withdrawn.

Allowability of Claims 16-20:

It should be noted that claims 16-20 were only rejected under 35 USC 112 and not under 35 USC 102 or 35 USC 103, thus, in light of the traversal of the 35 USC 112 rejections it is believed that claims 16-20 are now allowable.

First 35 USC 102 Rejection:

Claims 1, 8, 9, and 12-15 were rejected under 35 USC 102(e) as being anticipated by United States patent number 6,775,164 issued to Wong et al. This rejection is respectfully traversed.

Amended claim 1 calls for, among other things, coupling the bias current to a control electrode of the output

ONS000511  
PATENT

S.N. 10/685,094

transistor of the high voltage device to generate an output current. At least this element of amended claim 1 is not disclosed by the Wong et al reference. The Office Action indicates that transistors 124/20 are a high voltage device, transistor 20 is an output device, a transistor 42 is a switch, an initial bias voltage through 124 is shunted away from output transistor 20 by switch 42, and after an initial output voltage is reached output transistor 20 is turned on to generate an output current. However amended claim 1 indicates the high voltage device generates a bias current, the switch element shunts the bias current away from the output transistor, and the bias current is coupled to a control electrode of the output transistor of the high voltage device to generate the output current. Wong et al do not couple a bias current back to the control electrode of the output transistor (20). Thus, it is respectfully submitted that the relied on reference is deficient in anticipating amended claim 1.

Amended claim 8 includes, among other features, shunting the first current to an output of the startup circuit, using the first current to form an output voltage at the output of the startup circuit, and coupling a second current from an output of an output transistor to the output of the startup circuit to form the output voltage. Wong et al do not use the same output for shunting the first current to the output and for coupling the second current to the same output to form the output voltage. Wong et al shunt one current to output 47 (as stated in the Office Action) but steer the second current through transistor 20 and not to the same output 47.

Amended claim 9 depends from claim 8 and is believed to be allowable for least the same reasons as claim 8.

Claims 12 and 14 depend from amended claim 8 and are believed to be allowable for least the same reasons as claim 8.

Amended claim 15 includes, among other things, shunt the output current to the voltage return. The Office Action states

ONS000511  
PATENT

S.N. 10/685,094

that the Wong et al reference discloses that the output voltage and current (DC +) is returned at node 46 to disable the output by operating transistor 20. However, Wong et al do not shunt the output current (at DC+ per the Office Action) to the voltage return. Accordingly, it is respectfully submitted that amended claim 15 is not anticipated by the relied on reference.

Second 35 USC 102 Rejection:

Claim 15 was rejected under 35 U.S.C. 102(b) over United States patent number 5,477,175 issued to Tisinger et al. This rejection is respectfully traversed.

Amended claim 15 includes, among other limitations, generating a first output current at an output of a startup circuit responsively to a first value of an output voltage at the output of the startup circuit, and coupling the output of the startup circuit to a voltage return to shut the output current to the voltage return and disable the output voltage. This combination of limitations is not disclosed by the Tisinger et al reference. Tisinger et al generate an output voltage on output 112 (as stated in the Office Action), however, the circuit 105 does not disclose coupling the output (112 per the Office Action) of the startup circuit at which the output voltage is formed to the voltage return to shunt the output current to the voltage return. At least this combination of elements is not disclosed by Tisinger et al. Accordingly, it is respectfully submitted that the relied on reference is deficient in anticipating amended claim 15.

Claims 16-19 were not rejected under 35 USC 103 or 102 and were not rejected under either reference relied upon under this Office Action, thus, it is respectfully submitted that claims 16-19 are allowable.

Further, claim 16 calls for, among other things, coupling a bias current to the output. The Wong et al and Tisinger et

ONS000511  
PATENT

S.N. 10/685,094

al references do not disclose coupling a bias current and the first output current to the same output.

Also, claim 18 calls for, among other elements, enabling a pinch resistor to shunt the bias current. This element also is not disclosed by the Wong et al or Tisinger et al references.

The references cited but not relied upon were reviewed and are believed not to anticipate or make obvious applicants' invention.

ONS000511  
PATENT

S.N. 10/685,094

CONCLUSION

Applicant(s) made an earnest attempt to place this case in condition for allowance. In view of all of the above, it is believed that the claims are allowable, and that the case is now in condition for allowance, which action is earnestly solicited.

Two independent claims were added and one dependent claim was cancelled for a total of five independent claims and 19 total claims. The Commissioner is hereby authorized to charge any fees may be required or credit any overpayment to Deposit Account 50-1086.

If there are matters which can be discussed by telephone to further the prosecution of this Application, the Examiner is invited to call the undersigned attorney/agent at the Examiner's convenience.

Respectfully submitted,  
Frantisek Sukup et al., by

*Robert F. Hightower*

ON Semiconductor  
Law Dept./MD A700  
P.O. Box 62890  
Phoenix, AZ 85082-2890

Robert F. Hightower  
Attorney for Applicant(s)

Reg. No. 36163  
Tel. (602) 244-5603

Customer #: 27255